## *Remarks*

Applicant thanks the Examiner for the Examiner Interview conducted on February 19, 2004. Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 3-37 are pending in the application, with claims 3, 14, 16, 32, and 35 being the independent claims. Claims 3, 14, 32, and 35 are sought to be amended. Claims 1 and 2 are sought to be canceled without prejudice to or disclaimer of the subject matter recited therein. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding objections and rejections.

### *Restriction Requirement*

Claims 1 and 2 were previously withdrawn from consideration in response to a telephonic restriction requirement. By the current amendment, claims 1 and 2 are canceled without prejudice to or disclaimer of the subject matter recited therein.

### *Objections to the Claims*

In paragraph 1 of the Office Action, the Examiner objected to claims 1 and 35. The objection to claim 1 has been rendered moot by the cancelation of claim 1. Withdrawal of the objection to claim 1 is requested.

Regarding claim 35, the Examiner objected to the term, "...passed to gate-level implementation tools...." According to the Examiner, the term is "unclear to what applicant intend to mean within specification." Applicant respectfully traverses.

In claim 35, the term " passed to gate-level implementation tools" refers to a hand-off procedure described in the specification at, for example, (col. 3, line 64).

> "In a preferred embodiment, the ***hand-off*** between the RTL optimization system and the conventional back-end flow includes the RTL model along with chip and block level netlists, floorplans, routing, aspect ratios and areas, pin assignments, output loads, input, output and internal timing constraints, placement based wire loads for wires within and between partitions, and command scripts for controlling back-end tools. In this

> fashion, the back-end flow can be fully constrained to a single pass, thereby accomplishing true RTL level ***hand-off***." (Specification, page 7, paragraph 16)(emphasis added).

The term "...passed to gate-level implementation tools...." Is, therefore, believed to be unambiguous. Reconsideration and withdrawal of the objection is requested.

***Rejections under 35 U.S.C. § 102***

In paragraph 2 of the Office Action, the Examiner rejected claims 3-37 under 35 U.S.C. § 102(e) as being unpatentable over Dangelo, U.S. Patent No. 6,216,252, hereinafter, "Dangelo"). Applicant respectfully traverses.

The present invention is directed to the use of placement based information in designing integrated circuits. Placement based information, including, without limitation, placement based wire load models, are described throughout the specification. For example:

> "The RTL design methodology and system of the present invention uses ***placement based*** wire load models to capture the performance characteristics of the known physical implementations of individual partitions of an electronic design, and of the overall electronic design itself, prior to any logic synthesis. This performance data is used to optimize the partitioning, floorplanning, and routing of the electronic design in order to find a known solution to design goals. This solution defines the physical implementation of the electronic design at the partition and chip level and thus constrains the back-end flow so that only a single pass through conventional logic synthesis, place-and-route, and so forth is required. " (Specification at pages 6 and 7, paragraph 15) (emphasis added).

> "The performance data preferably quantifies the relationship between the area, circuit delay, and output load of the logic structure for a number of different physical implementations. ***This performance data is created by placing and routing each physical implementation*** to create a placement based wire load model." (Specification at page 8, lines 4-7) (emphasis added).

Placement based information is thus derived from physical implementations rather than estimations or statistics. Accordingly, independent claims 3, 14, 16, 32, and 35 recite, among other features, placement based information. For example:

"using placement based information," (claim 3);
"creating a virtual prototype using placement based information," (claim 14);
"each logic building block having performance data based on placed and routed implementations of that logic building block," (claim 16);
"monitoring area and placement based performance data," (claim 32; and
"each logic structure having performance data based on placed and routed implementations of that logic building structure," (claim 35.

Dangelo teaches to use statistical or estimated information rather than placement based information. For example:

> "As will become evident hereinafter, partitioning the design at a high level (behavioral description) into architectural blocks creates a 'vehicle' for providing such structural information at the behavioral description level, thereby adding the ability to ***estimate lower-level physical parameters***. Further, partitioning helps the designer explore other avenues such as operator level parallelism and process level concurrency in order to improve the design." (Dangelo at col. 8, lines 54-61) (emphasis added).

> "For more accurate analysis, it might be necessary to use a floor-planner or placement and routing programs to ***estimate wire delays***. The wire delays are then back annotated into the design database prior to simulation." (Dangelo at col. 11, lines 49-52) (emphasis added).

> "In the loop shown: for larger functional blocks, a floor planner 710 is used for placements and more accurate wire delay prediction 712 and, with this information, using the more accurate block size provided by the floor planner to ***re-estimate the internal wire delays*** of the lower level functional units and back-annotating these delays into the Design Compiler to provide more meaningful internal timing optimization." (Dangelo at col. 14, lines 3-11) (emphasis added).

Dangelo, thus, does not teach or suggest, using placement based information as recited in the pending claims. Reconsideration and withdrawal of the rejection of independent claims 3, 14, 16, 32, and 35, and the claims dependent therefrom is requested.

## *Conclusion*

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding objections and rejections.

Applicant believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Patrick E. Garrett
Attorney for Applicants
Registration No. 39,987

Date: 2/20/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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